CPT-DD28035 Card

Dual TMS320F28035 MCU Controller Card

Technical Brief

June 2014
Manual Release 1.1
Card Version 1.1

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CPT-DD28035 Manual Revision History

CARD VERSION 1.0: Initial Board for prototype purposes.

Release 1.0 – Initial Release

CARD VERSION 1.1: Board Updated for General Use

Release 1.1 – Updates to match board revision changes

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CPT-DD28035 Dual MCU Controller Board

1.0 Overview of the CPT-DD28035

The CPT-DD28035 is a low cost standardised dual MCU controller board designed to provide a fully flexible interface between dual TMS320F28035 MCUs and a user customised motherboard. The board has been designed to meet different user interface requirements whilst providing a 4 layer MCU core with basic on-board functionality. The board is compatible with the DD Series range of motherboards.

The board is based around two Texas Instruments TMS320F28035PN MCUs, which have been specifically developed for use in digital motor/motion control applications.

The CPT-DD28035 card measures 115mm x 75mm.

On-card facilities include:

- 2 off TMS320F28035PN "Piccolo" Microcontrollers, each containing:
  - 64k x 16 Flash
  - 1k x 16 OTP ROM
  - 8k x 16 Boot ROM
    - Software Boot Tables
    - Standard Math Tables
  - 10K x 16 Single Access RAM (SARAM)
    - L0: 2 Blocks of 2K x 16 Each DPSARAM
    - L1 and L2: 2 Block of 1K x 16 DPSARAM
    - L3: 1 Block of 4K x 16 Each DPSARAM
    - M0 and M1: 2 Blocks of 1K x 16 SARAM
  - Control Law Accelerator
  - Internal Temperature Sensor – for measuring MCU Junction Temperature
- Serial Flash Memory with 1Mbit of non-volatile storage
- 1 off Power LED
- 4 off Status LEDs
- Reset/Power-On Circuitry
- Power supply to generate all on-card supplies
- Power supply operation from input 12VDC

The card also supports the following peripheral interfaces:

- JTAG interface shared between MCU
- 1 off 3.3V-TTL serial interface per MCU
- 1 off 28-way Connector with:
  - 2 off 3.3V-TTL Enhanced Controller Area Network (eCAN) Bus interfaces
  - 4 off (selectable) Serial Communications Interfaces
  - Enhanced Pulse Width Modulator (ePWM) interfaces
  - Selectable Interrupt Sources
- 2 off 26-way Connectors with:
  - 16 off 12-bit 0-3.3V ADC inputs
  - 3.3V Analog Reference Voltage

Figure 1-1 shows a functional block diagram of the CPT-DD28035 card, illustrating all major sections.

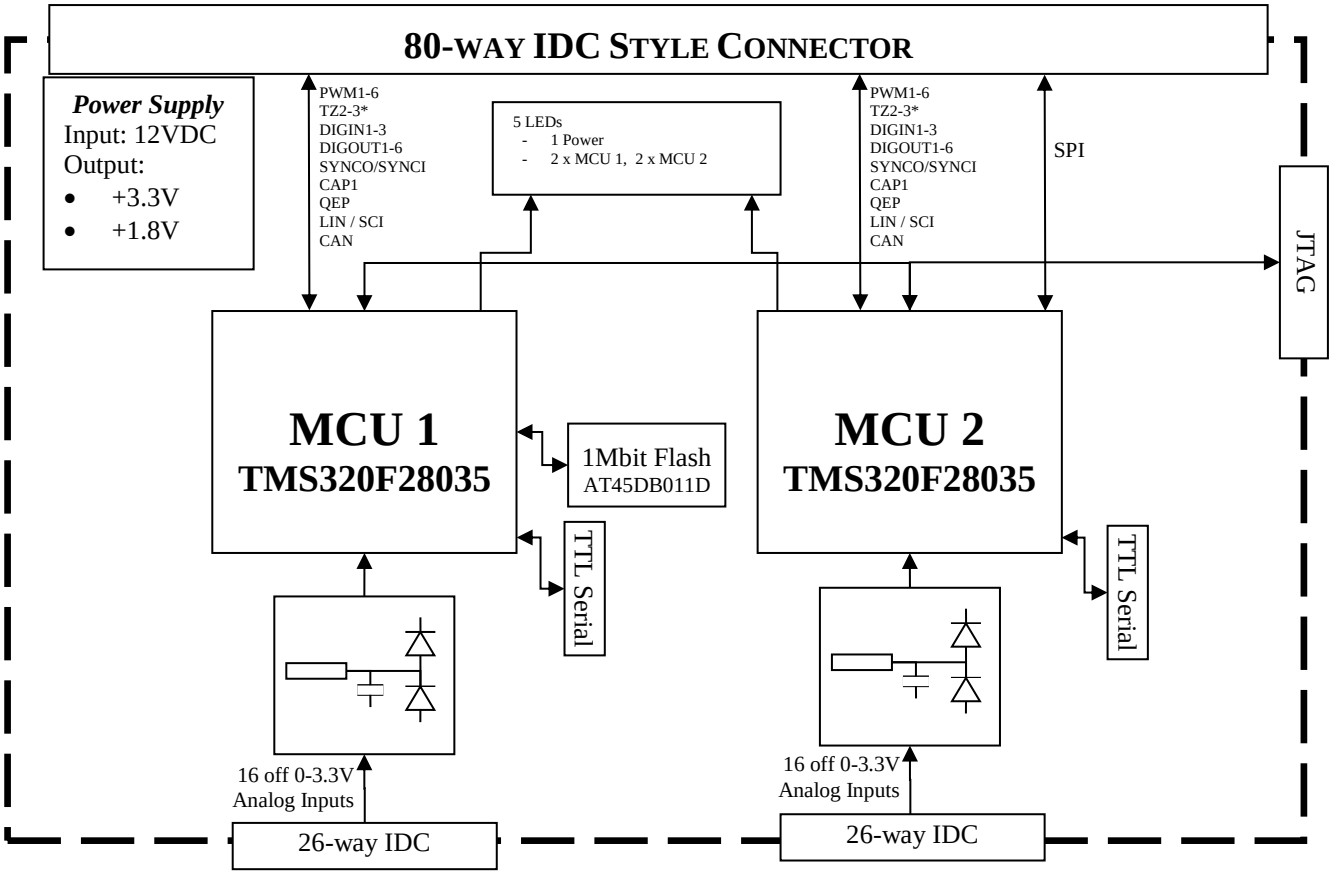

Figure 1-1: Functional Diagram of CPT-DD28035 Controller Board

1.1 Digital I/O

The CPT-DD28035 card supports a maximum of 64 bits of 3.3V-TTL digital I/O, depending on the user defined configuration of each MCUs pins.

All but 2 of the TMS320F28035's digital I/O pins can operate in either a "Digital I/O or "Peripheral I/O" mode. The user must select the correct mode of operation for each pin within their software. Many of the Digital I/O pins are intended to be operated only in their Peripheral I/O mode.

1.2 Analog Inputs

Each TMS320F28035 MCU has 16 off ADC inputs that accept voltages in the range of 0-3.3V. The analog inputs are divided into two banks of 8 (ADCINA0-7 and ADCINB0-7). Each bank feeds into an 8 to 1 analog multiplexer with a sample and hold circuit. The outputs from the two sample and hold circuits are fed directly into a single 12-bit ADC Module. The ADC Module's "… basic principle of operation is centred around the configurations of individual conversions…"[I]. This enables the single conversion or a single channel to be configured rather than the sequencer based ADCs that were used in previous 28x processors which required setting up a stream of conversions.

The maximum total conversion time for each ADC input is 13 ADC Clock ticks (216.67ns @ 60MHz ADC Clock).

The CPT-DD28035 analog inputs provide 32 off filtered external inputs separated into two groups of 16. Each group of 16 is fed to a separate TMS320F28035 MCU.

It is strongly recommended that the ADC be software calibrated for both gain and offset. Please consult the Texas Instruments documentation on the ADC converter for further information. *TMS320x2802x, 2803x Piccolo Analog-to-Digital Converter (ADC) and Comparator Reference Guide*, Literature Number: *SPRUGE5F*.

The 32 off filtered analog inputs are available on dual 26-way IDC headers, with each header corresponding to one MCU. Each input has a low pass or "glitch" filter and a diode clamp circuit before being fed into the MCU. The board accepts 0-3.3V inputs for these circuits.

A 3.3V Analog reference is available on each 26-way header for use off card. It is recommended that this reference be fed into an off-card op-amp circuit for external buffering rather than being used directly.

1.3 Gate Drive Interface

The TMS320F28035 MCU supports 14 PWM channel outputs, made up of 7 complementary pairs with programmable deadbands. The MCU chip has 7 enhanced pulse width modulator (ePWM) modules. Each module consists of "… one complete PWM channel composed of two PWM outputs: EPWMxA and EPWMxB"[II]. Dead band compensation is required to be software-calculated for the simple compare outputs. In addition the 'A' channel of each PWM module can be operated with increased precision control of the PWM output, which is referred to as the High-Resolution Pulse Width Modulator (HRPWM). This "… extends the time resolution capabilities of the conventionally derived digital pulse width modulator"[III].

Each ePWM module can be connected together via a clock synchronization scheme that enables them to operate as a single system. The system can be extended to include the capture peripheral modules (eCAP).

[I] *"Piccolo Microcontrollers"* – Literature Number: SPR584G, Texas Instruments March 2012

[II] *"TMS320F2802x, 2803x Piccolo Enhanced Pulse Width Modulator (ePWM) Module Reference Guide"* – Literature Number: SPRUGE9E, Texas Instruments Revised March 2011.

[III] *"TMS320F2802x, 2803x Piccolo High Resolution Pulse Width Modulator (HRPWM) Module Reference Guide"* – Literature Number: SPRUGE8E, Texas Instruments Revised October 2011

Gate fault signals are fed back to the MCU via the Trip-Zone TZ2* and TZ3* pins. These signals act as interrupts that can be configured to act on any or all of the EPWMxA or EPWMxB pins. This enables an MCU hardware interrupt trip to immediately occur on detection of a fault, thus disabling the PWM signals within 2 clock cycles using hardware logic internal to the MCU.

1.4 Communications

The CPT-DD28035 controller board supports four off non-isolated 3.3V-TTL serial communications interfaces (SCI / LIN), two 3.3V-TTL synchronous serial peripheral interfaces (SPI) and two off 3.3V-TTL enhanced Controller Area Network (CAN) bus interfaces.

The high-speed synchronous serial peripheral interfaces can be used to communicate to other computer systems. The interfaces can support either master or slave protocol, selected by software. The SPI interface on MCU2 is available via the 80 way external connector and the MCU1 SPI interface is used for the on-card Flash Memory chip.

The 3.3V-TTL serial port can be used to communicate to a terminal emulation program, via an interface board, to aid in program development. There are separate SCI connectors for each MCU on-card. All signal conditioning for for CAN, LIN or SCI interfaces is to be carried out off-card. The signals are all made available unbuffered on the CPT-DD28035. The MCU2 SPI interface has series resistance included to aid with high speed operation.

1.5 On-card memory

The CPT-DD28035 controller board supports 64k x 16bit of on-card Flash, 10k x 16bit of SARAM and 8k x 16 Boot ROM per MCU. Programs can be directly executed from RAM, via the JTAG interface or from Flash. By default, the card runs programs from the flash memory.

In addition to the on-chip memory the CPT-DD28035 has a 1Mbit SPI interfaced Flash Memory chip for external data storage interfaced via MCU1.

1.6 Power Supply

The standard CPT-DD28035 controller board has an on-card voltage regulator chips that accept an input voltage of +12VDC and produce +3.3V and +1.8V voltages.

Analog supplies are generated via an LC filter from the digital +3.3V supply and this supply is also available on the external 26 way analog connectors.

1.7 JTAG/programming

The CPT-DD28035 controller board has a JTAG interface for programming the MCU's Flash ROM or RAM. This port can also be used for emulator/debugging purposes using the Code Composer Studio Pod.

The JTAG has been configured to operate with both MCUs located on the CPT-DD28035 board.

2.0 Specifications

2.1 Controller MCU Section

Processor	Texas Instruments TMS320F28035PN
Quantity	2
On-card Memory (per MCU)	64k x 16 Flash Memory 10k x 16 RAM 8k x 16 Boot ROM 1k x 16 OTP ROM
Reset	120ms hardware reset generated on-card from power up and supply failure. Can also be triggered for MCU1 on **X1.6** or MCU2 on **X1.42**
Non-Volatile Memory Storage	1Mbit of memory storage using an SPI flash ROM chip Accessed via SPI interface on MCU1
Interrupts	Support for 2 off Gate Driver interrupts (TZ2*, TZ3*) per MCU Note: All GPIO0-31 inputs can be configured as MCU Interrupts

2.2 Analog Inputs

Number of Channels	32 single ended
A/D Resolution	12 bits
A/D Conversion Time	216.67ns (@60MHz ADCCLK) + Sample Window setting
Number of ADC's	1 (8 channels are multiplexed on-chip to form a bank)
Number of S/H units	2 (each bank has one sample and hold unit)
Reference Voltage	Internal

2.2.1 AC General Inputs

Definition	32 off 0-3.3V analog inputs with low pass filter capacitors MCU1: 1ADCINA0-7, 1ADCINB0-7 MCU2: 2ADCINA0-7, 2ADCINB0-7 Channel 1ADCINA5 can be configured for internal junction temperature measurement.
Input Voltage Range	0-3.3V maximum
Dynamic Response	Cut-off frequency >150kHz
PCB Connections	26-way IDC header MCU1: **X5**, MCU2: **X6**

2.3 Digital I/O

Definition	64 bits total **MCU1 and MCU2** GPIO0-11, GPIO40,41 (shared with EPWMxA – EPWMxB) GPIO13 GPIO14 (shared with LINTXA) GPIO15 (shared with LINRXA) GPIO16-17 (shared with interrupts TZ2* and TZ3*) GPIO20-23 (shared with EQEP interface) GPIO24 (shared with Capture Port) GPIO28-29 (shared with SCIA port) GPIO30-31 (shared with eCAN bus) GPIO32,33 (shared with SYNCI/O) **MCU2 only** GPIO12,25,26,27 (shared with SPI interface)
Digital high input voltage threshold	+2.4V
Digital low input voltage threshold	+0.4V
Digital outputs rated at	±4mA per bit, ABSOLUTE MAXIMUM ±8mA for Group 2 pins (GPIO16-19)
PCB Connection	MCU1:GPIO28-29 4-way MOLEX header (**X3**) MCU2:GPIO28-29 4-way MOLEX header (**X4**) All other I/O available on 80-way IDC header (**X1**)

2.4 PWM Gate Drive Interface

Definition (per MCU)	Seven enhanced PWM Modules (ePWM) that can provide: • 14 EPWM outputs, or • 7 HRPWM outputs
ePWM Outputs	Each ePWM Module consists of two PWM outputs (EPWMxA and EPWMxB) with programmable deadband generation that can be configured as: • Two independent PWM outputs with single-edge operation • Two independent PWM outputs with dual-edge symmetric operation • One independent PWM output with dual-edge asymmetric operation
HRPWM Outputs	Increased resolution capacity using the EPWMxA channel.
Gate Fault Interrupt	Programmable trip zone allocation of both cycle-by-cycle trip and one-shot trip on fault conditions. The PWM signals are placed into a high impedance state.
Output Voltage	0-3.3V
PCB Connections	80-way IDC header (**X1**)

2.5 Communications Interface

Definition	The TMS320F28035 has one off serial communication interface port (SCI), one off LIN serial communications interface, two off serial peripheral interfaces (SPIA and SPIB) and an enhanced controller area network port (eCAN)
Compatibility	Serial Communications Interface (SCI) is at LVTTL levels via on-card 4 way connectors to maintain compatibility with the CPT-COM range of interfaces.
Configuration	**DEFAULT** modes • SCI set as a 3.3V-TTL level serial port accessing SCIA, • LIN set as Digital I/O • SPIA set as Digital I/O • MCU1: SPIB set as SPI for On-card Serial Flash • MCU2: SPIB set as Digital I/O • eCAN set as digital I/O
Isolation	None

2.5.1 Serial Communication Interface – SCI

Definition	Two-wire asynchronous serial port (UART) that supports a 4-level, receive and transmit FIFO for reducing servicing overhead. The receiver and transmitter are double buffered with separate enable and interrupt bits. The SCI port on each MCU is available via the 80 way IDC header or alternatively on a 4 way MOLEX connector located next to the MCU.

2.5.1.1 Serial Communication Interface – MCU1 and MCU2 SCIA

Definition	This provides a 3.3V-TTL level serial connection, with two pin serial communications for interface to an off-card 3.3V-TTL level to RS-232 translation card. This is necessary for interfacing to a standard PC serial port.
Communications Port	SCIA
Current Limit	±50mA
PCB Connections	MCU1: 4-way MOLEX header with VCC (+3.3V) and GND connections (**X3**) Also available on 80-way IDC header **X1** pins 19 (SCITXA) and 20 (SCIRXA) MCU2: 4-way MOLEX header with VCC (+3.3V) and GND connections (**X4**) Also available on 80-way IDC header **X1** pins 55 (SCITXA) and 56 (SCIRXA)

2.5.1.2 Serial Communication Interface – MCU1 and MCU2 LINA

Definition	This provides a 3.3V-TTL level serial connection, with two pin serial communications for interface to an off-card 3.3V-TTL level to RS-232 translation card. This is necessary for interfacing to a standard PC serial port
Communications Port	LIN
Current Limit	±50mA
PCB Connections	Available on 80-way IDC header **X1** pins 14 (MCU1:LINTXA), 15 (MCU1:LINRXA), 50 (MCU1:LINTXA) and 51 (MCU1:LINRXA).

2.5.2 Serial Peripheral Interface – MCU1: SPI

Definition	Four-pin serial peripheral interface (SPI) module. It is a high speed, synchronous serial I/O port that allows a serial bit stream of programmed length (one to sixteen bits) to be shifted into and out of the device at a programmable bit-transfer rate **DEFAULT MODE:** Configured as SPI
Compatibility	4 wire SPI mode
PCB Connection	Used by AT45DB011D Serial Flash chip

2.5.3 Serial Peripheral Interface – MCU2: SPI

Definition	Four-pin serial peripheral interface (SPI) module. It is a high speed, synchronous serial I/O port that allows a serial bit stream of programmed length (one to sixteen bits) to be shifted into and out of the device at a programmable bit-transfer rate Available on MCU2 **DEFAULT MODE:** Configured as digital I/O pins
Compatibility	4 wire SPI mode
PCB Connection	Available on 80-way IDC header **X5** pins 76 (SCLK), 77 (SOMI), 79 (SIMO) and 17 (/CS)

2.5.4 Enhanced Controller Area Network Module – eCAN

Definition	eCAN bus module which supports up to 1Mbps transfer
Compatibility	Fully compliant with CAN protocol version 2.0B
PCB Connections	Available on 80-way IDC header **X1** pins 17 (MCU1:CANTX), 18 (MCU1:CANRX), 53 (MCU2:CANTX) and 54 (MCU2:CANRX)

2.6 JTAG

Definition	MCU interface connection, which enables the two TMS320F28035 MCUs to interface to an ICE to provide a real-time debugging environment
Compatibility	Compatible with IEEE 1149.1 standard for scan-based emulation
PCB Connection	14-way IDC connector (**X2**)

2.7 Software

Standard Support Software	Monitor Program, standard library source code, sample programs Texas Instruments: Code Composer Studio V5 and above

2.8 General

Physical Dimensions	L: 75mm
	W: 115mm
	H: 11mm approx.
Mounting Arrangement	2 off 3.5 mm holes spaced 105mm apart at the bottom corners of the board 80-way IDC header can also be soldered into the motherboard to provide additional support
Environmental	-40 – 85°C ambient operating temperature 5% - 95% non-condensing humidity

2.9 Power Supply

Input Voltage Range	8 – 24VDC Absolute Maximum +12VDC nominal
Standalone Input Current	**20-50mA** (depending on the active sections within the MCU)
Max Input Power	Approx. **TBD ~500mW**
Supplies Generated on-card	+3.3V Digital
	+1.8V MCU Core
Input Power Connector	80-way IDC Connector (**X1**) +12V) on pins 1-2, GND on pins 3-4

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Appendices

Appendix A Component Layout

Top Layer